

FIG. 1

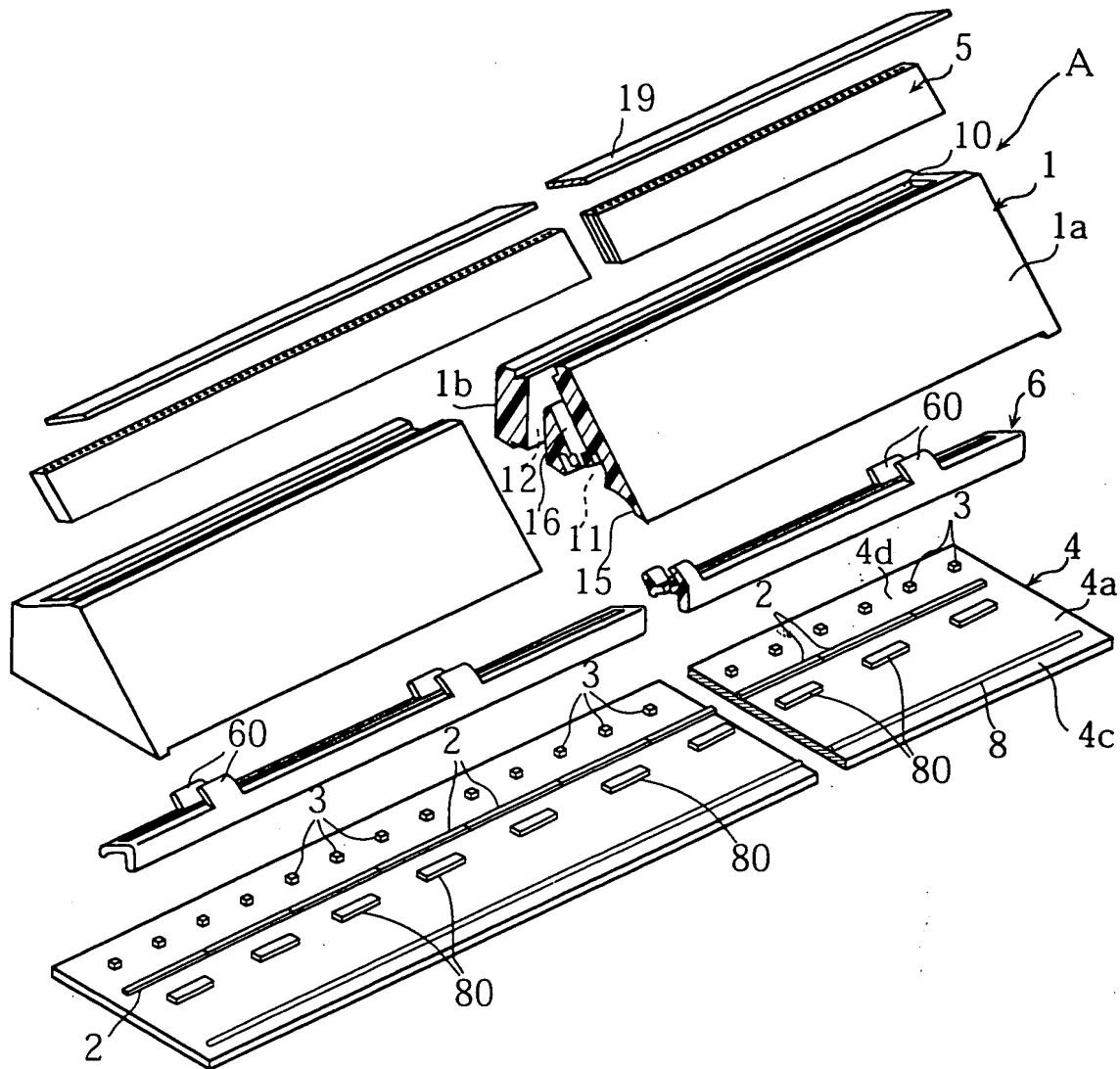


FIG.2

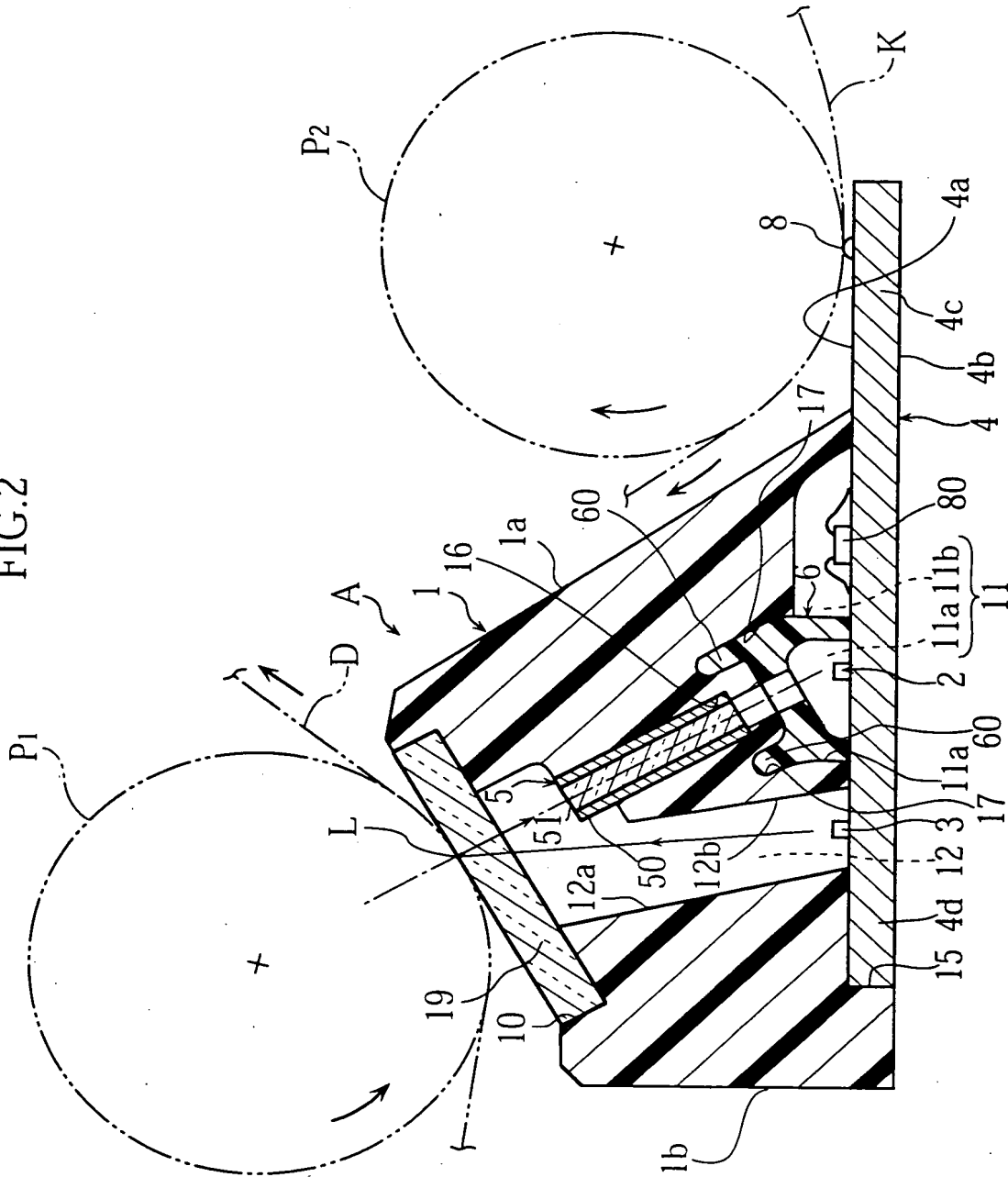


FIG. 3

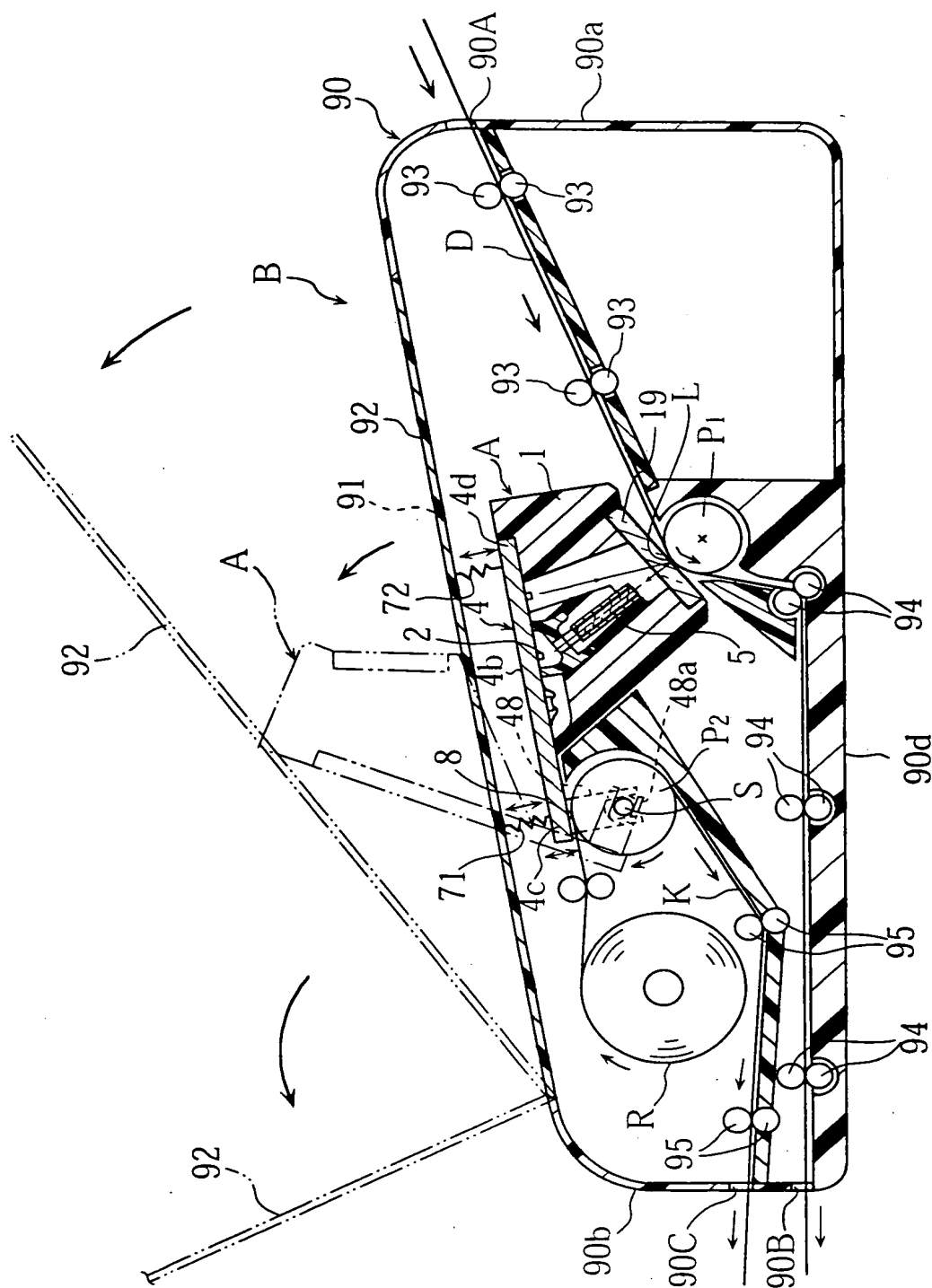


FIG.4

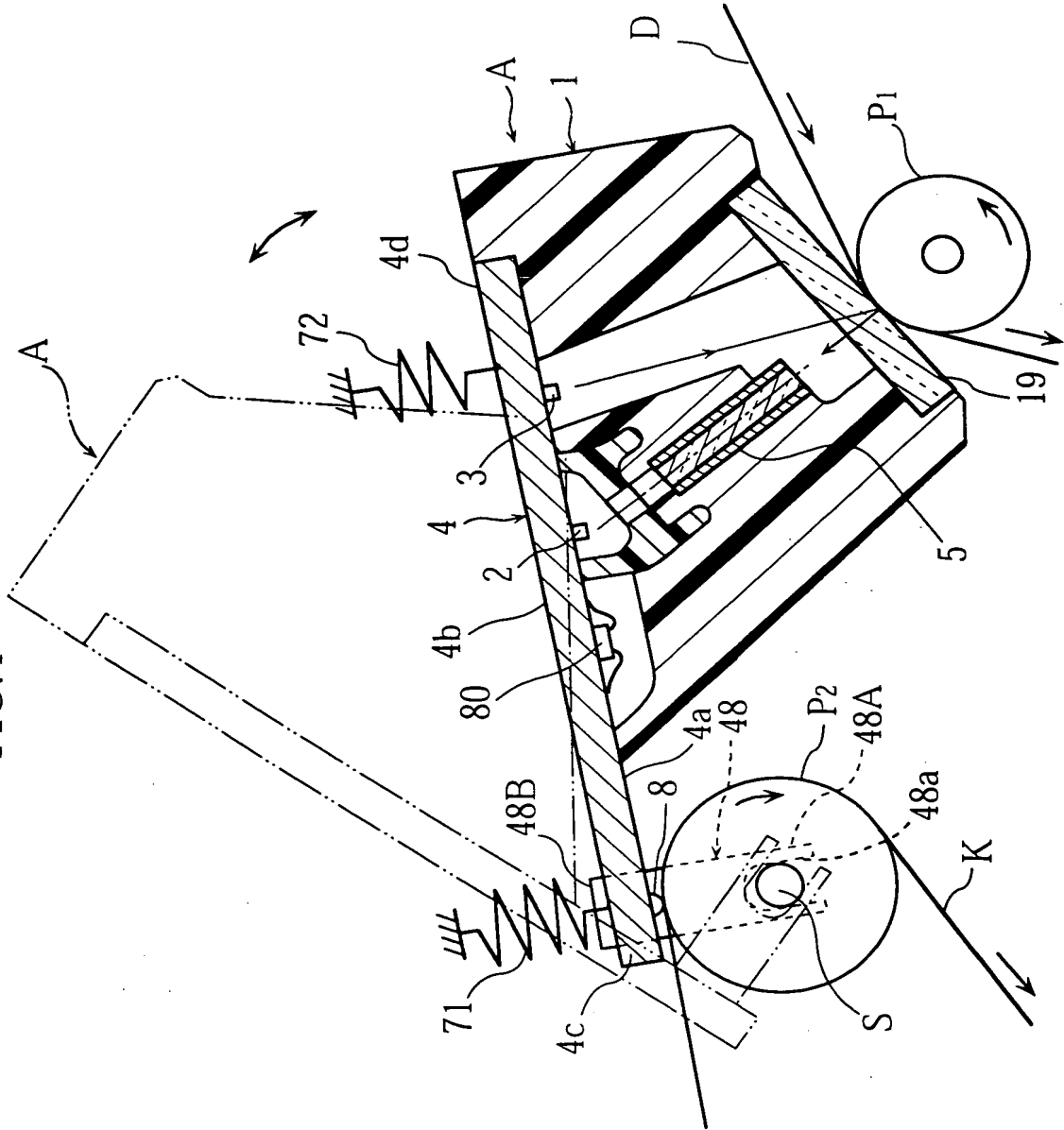


FIG. 5

FIG. 5

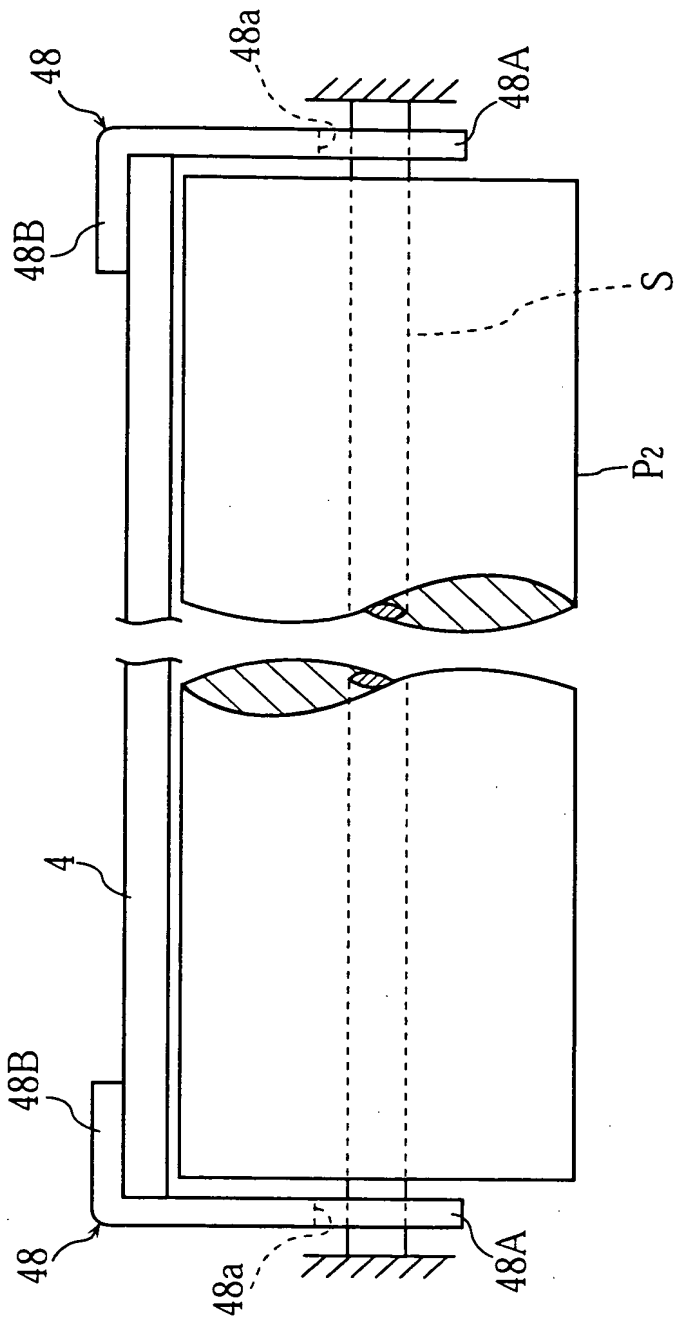


FIG. 6

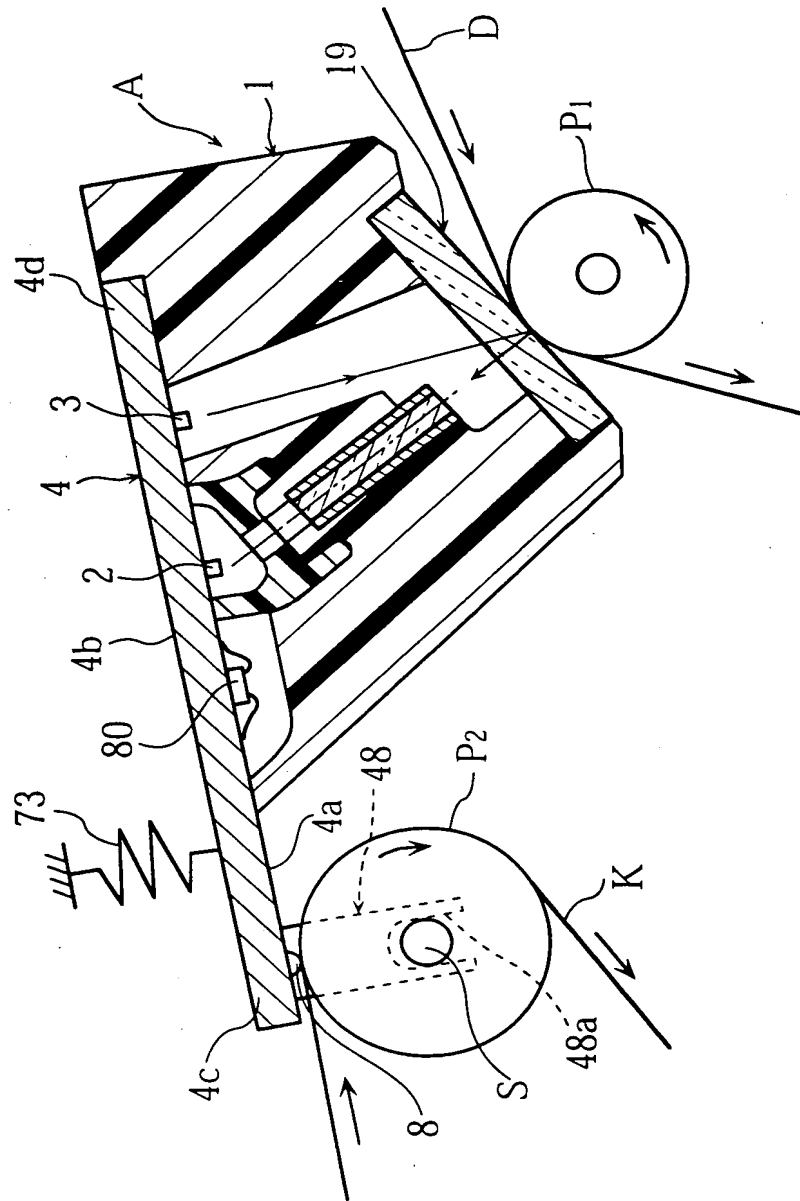


FIG. 7

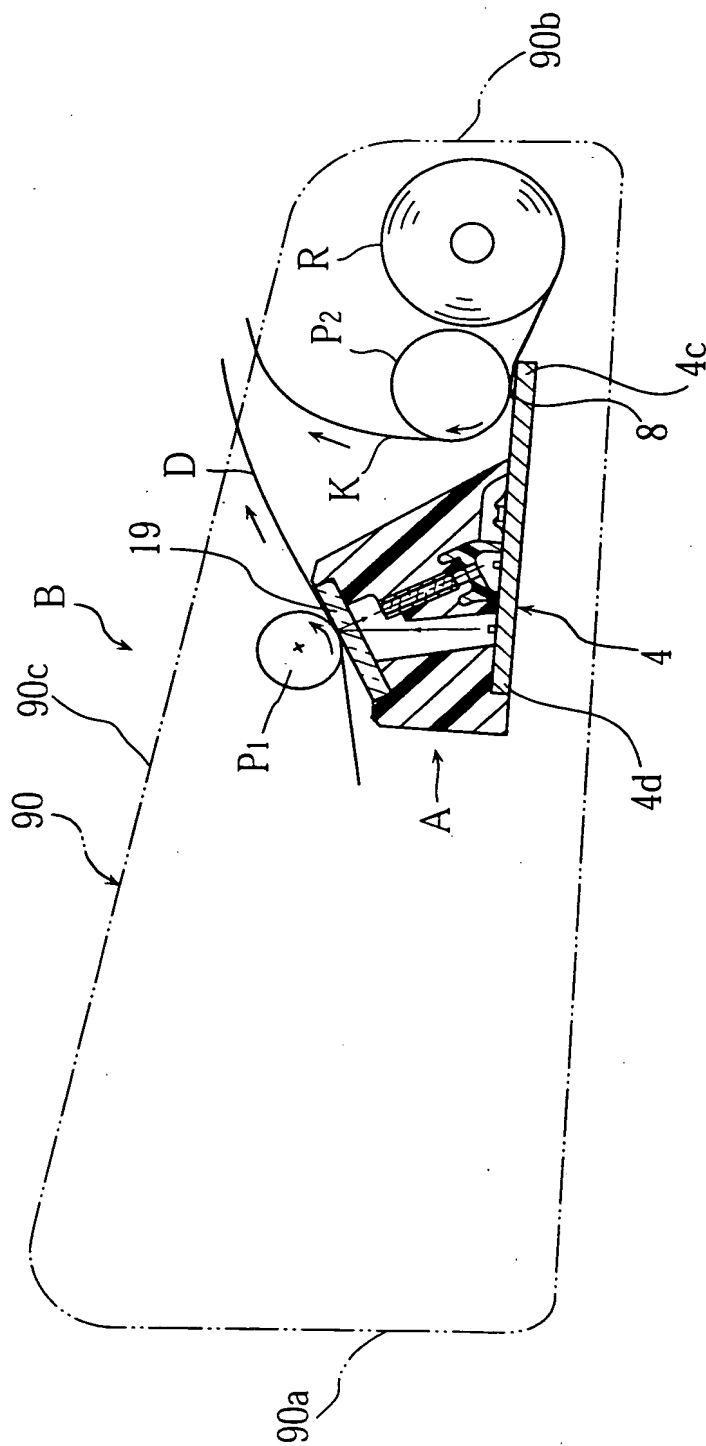


FIG. 8

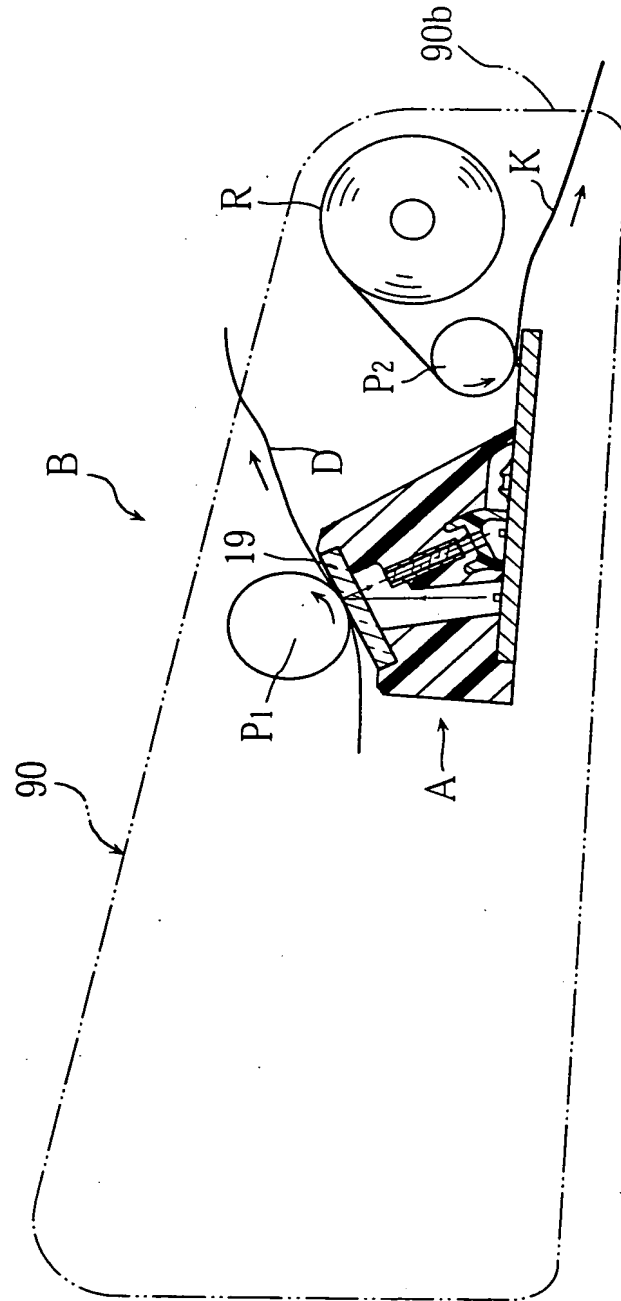


FIG.9

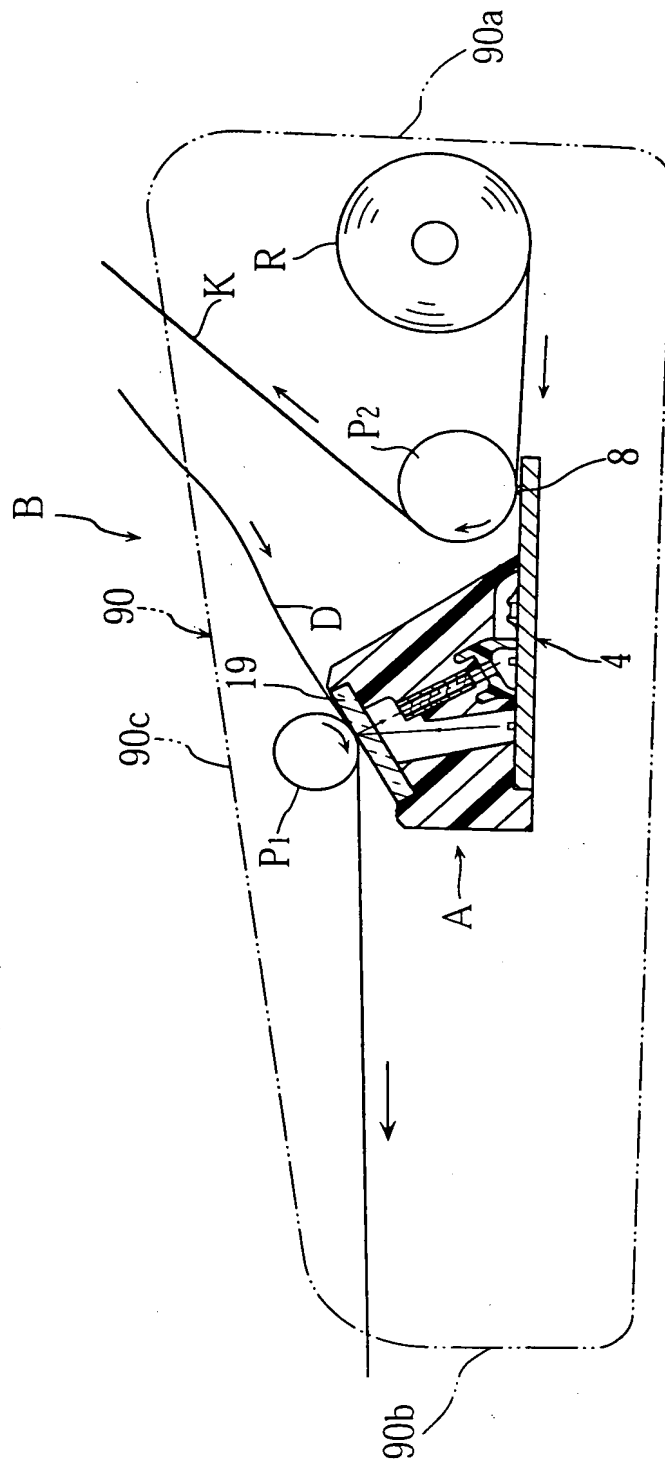


FIG.10

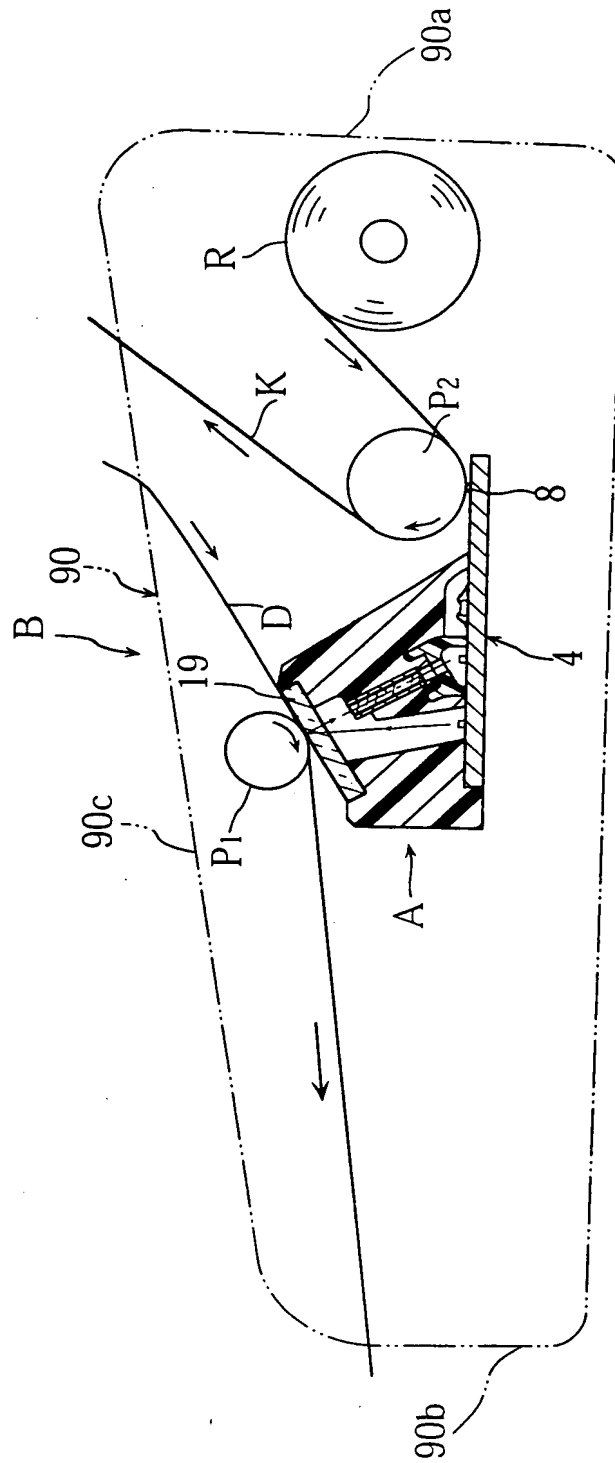


FIG.11

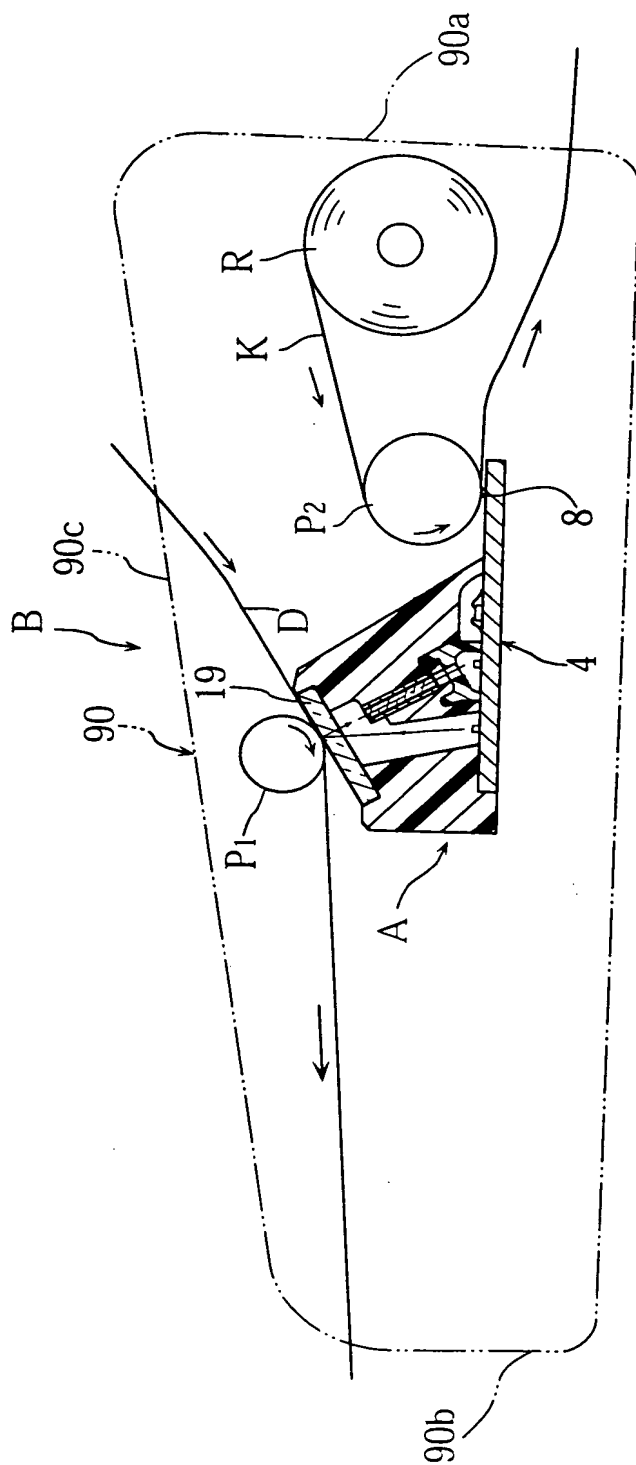


FIG.12

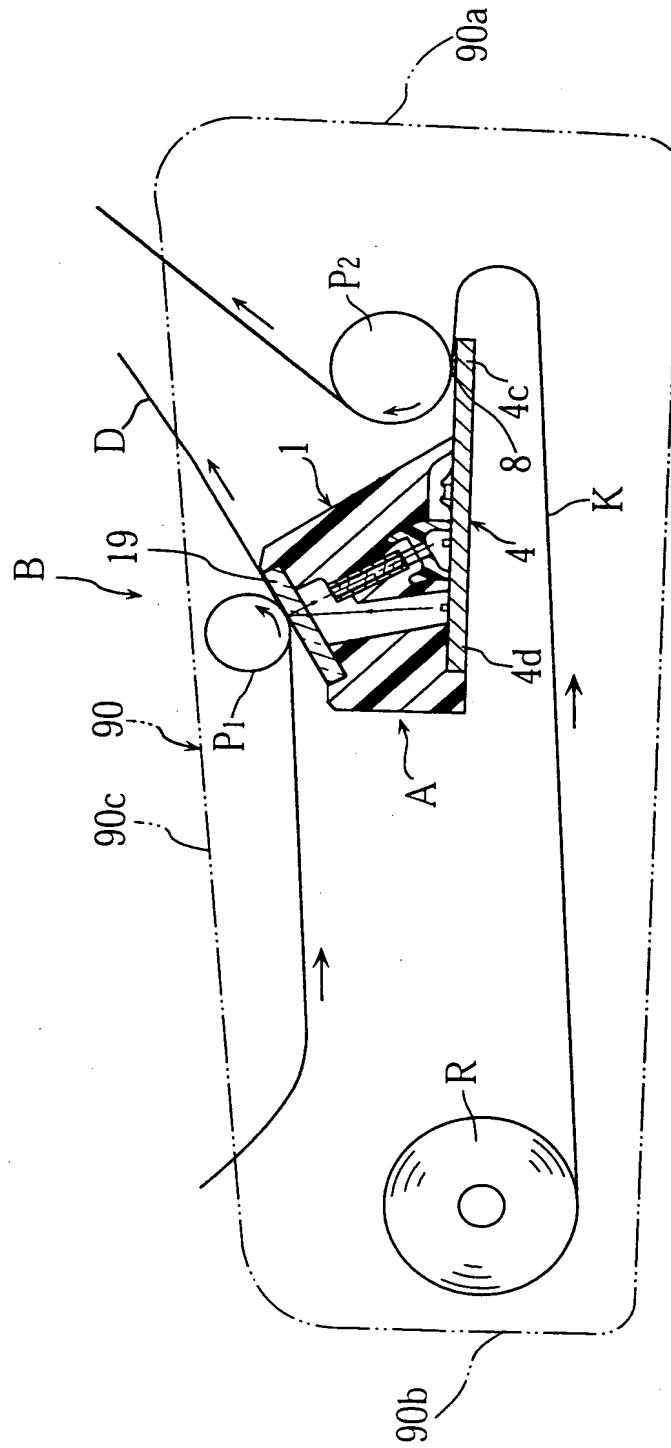


FIG.13

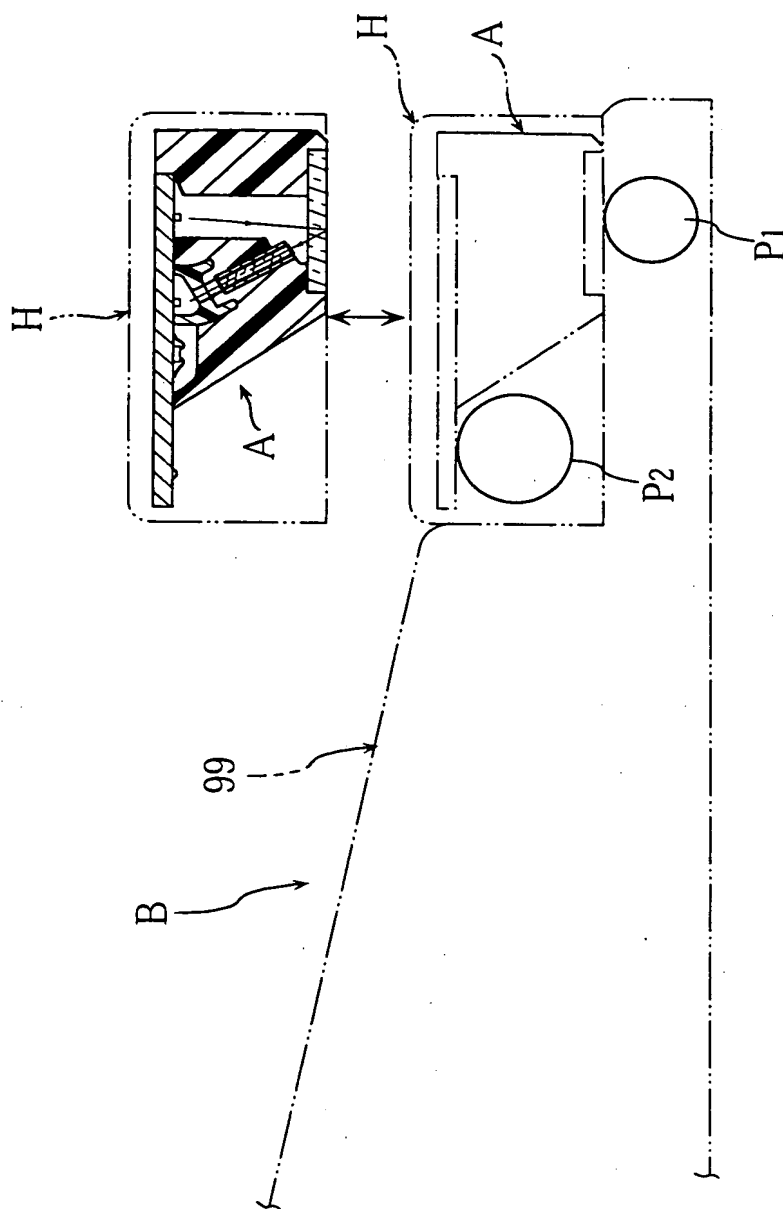


FIG.14

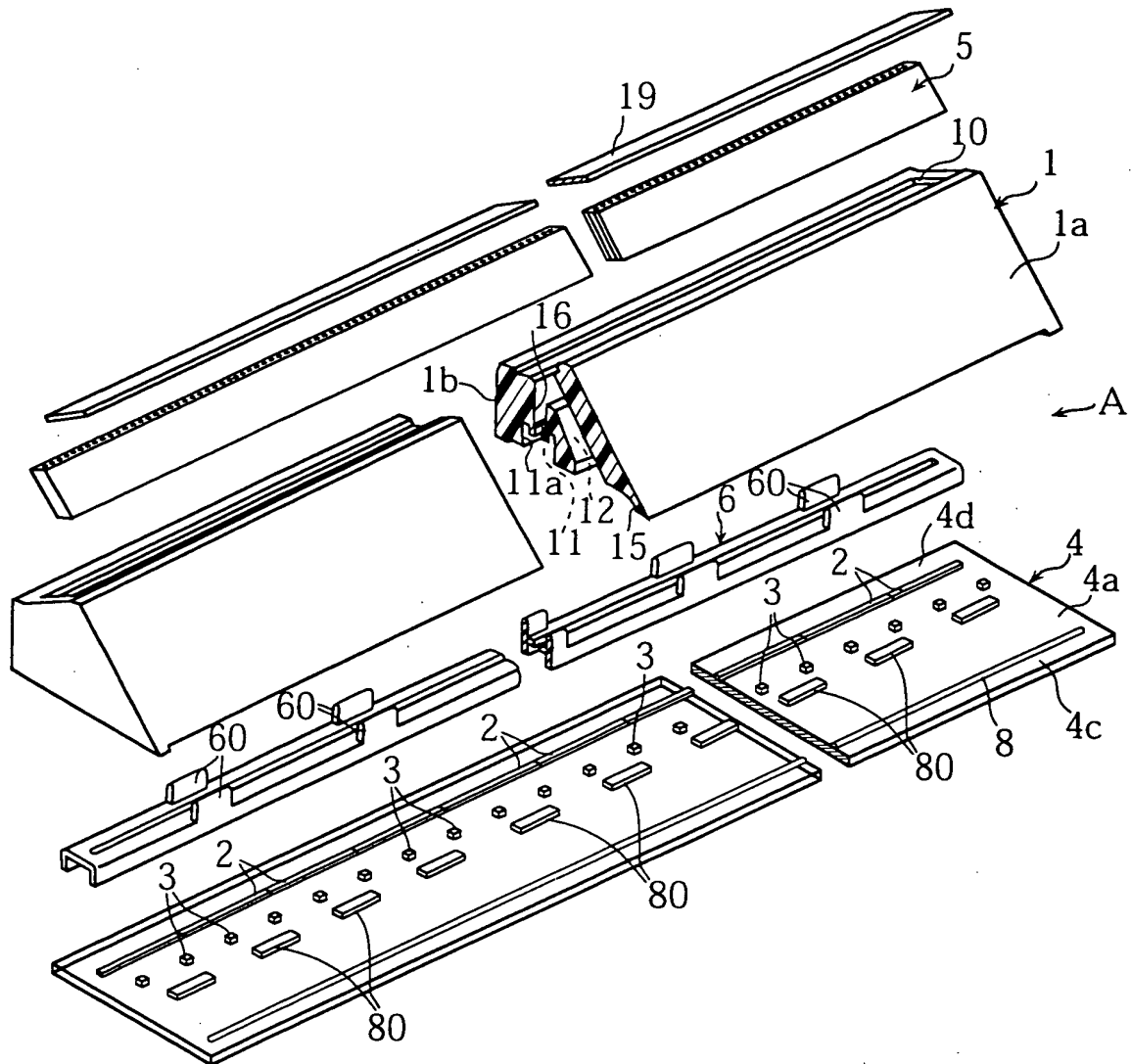
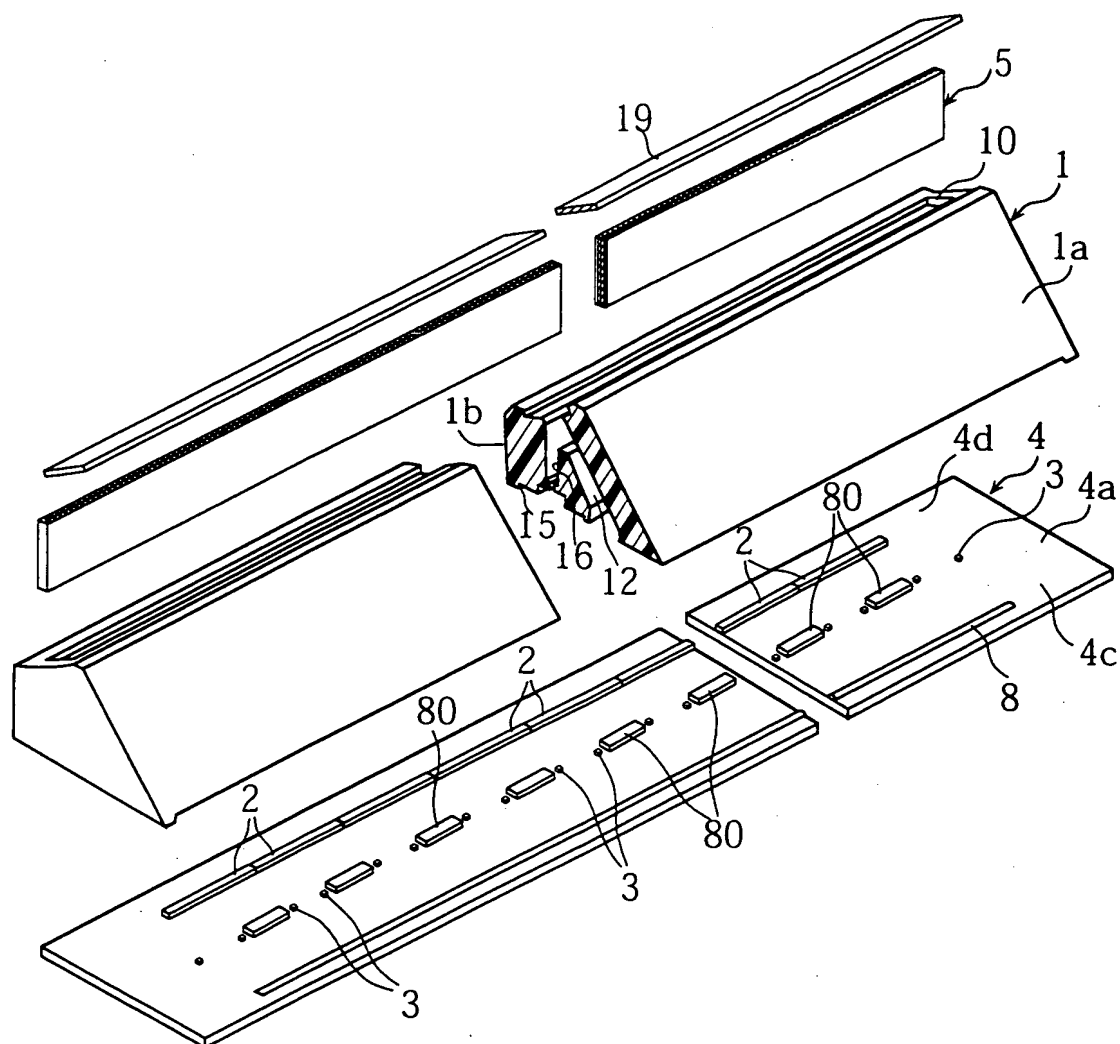
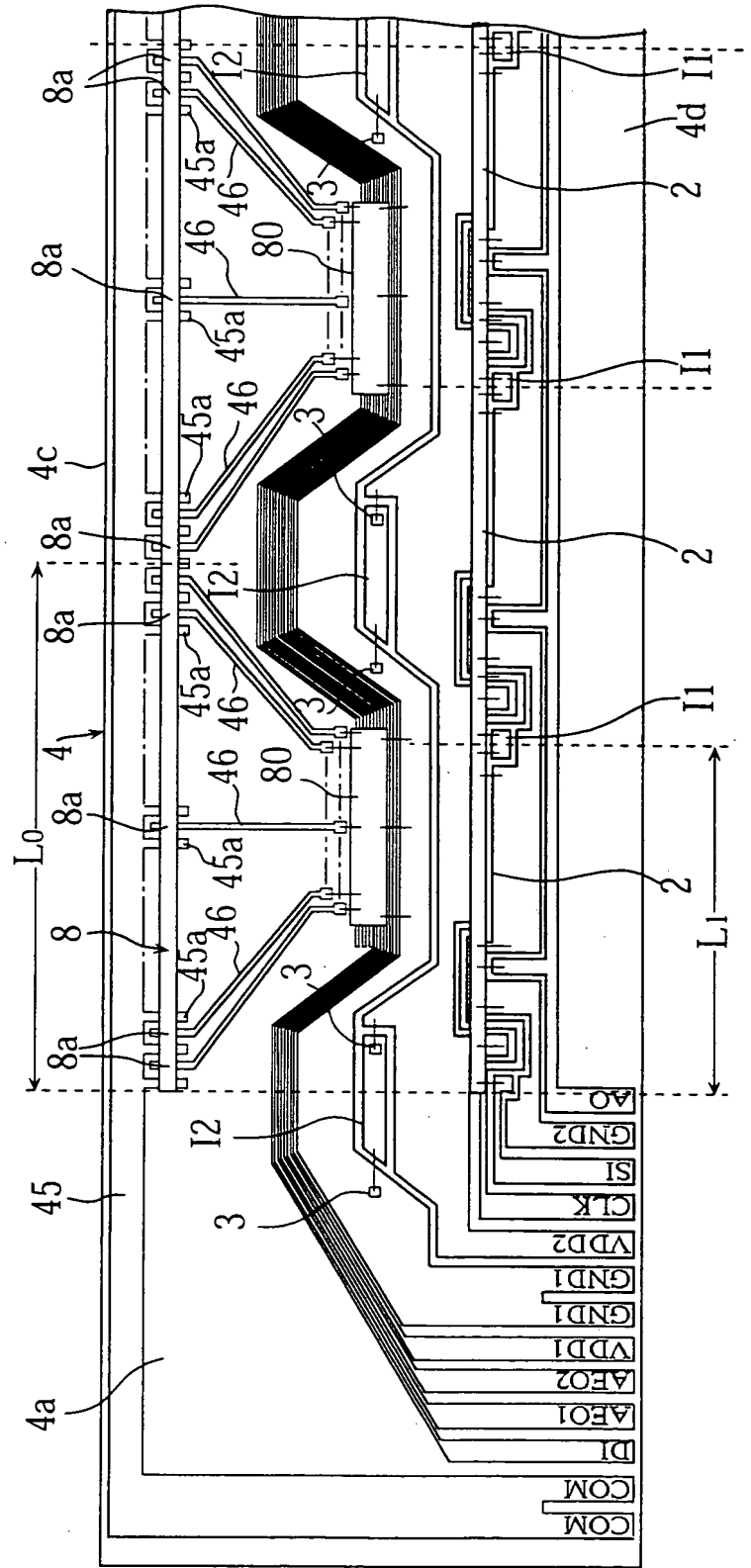


FIG. 16



A detailed cross-sectional diagram of a semiconductor device. The base is a substrate labeled 8, which has three distinct regions: 4c on the left, 4b in the middle, and 4d on the right. On top of the substrate are several components: a layer 15 on the far left; a central structure consisting of a lower layer 16 and an upper layer 5, separated by a vertical interface 2; another layer 11 on the right side of the central structure; and a thin layer 80 covering the entire top surface. A large, hatched wedge-shaped region 1 is positioned over the central part of the device. This wedge has a sloped front face 1a and a rear face 12. Inside the wedge, there is a horizontal layer 19 and a vertical feature 51. To the left of the wedge is a circular area P₁, and to the right is a larger circular area P₂. A dashed line L indicates a boundary or path near the left edge of the wedge. Other labels include 10, 1b, 3, 4, and K.

FIG. 19



TOP OF SHEET

FIG.20

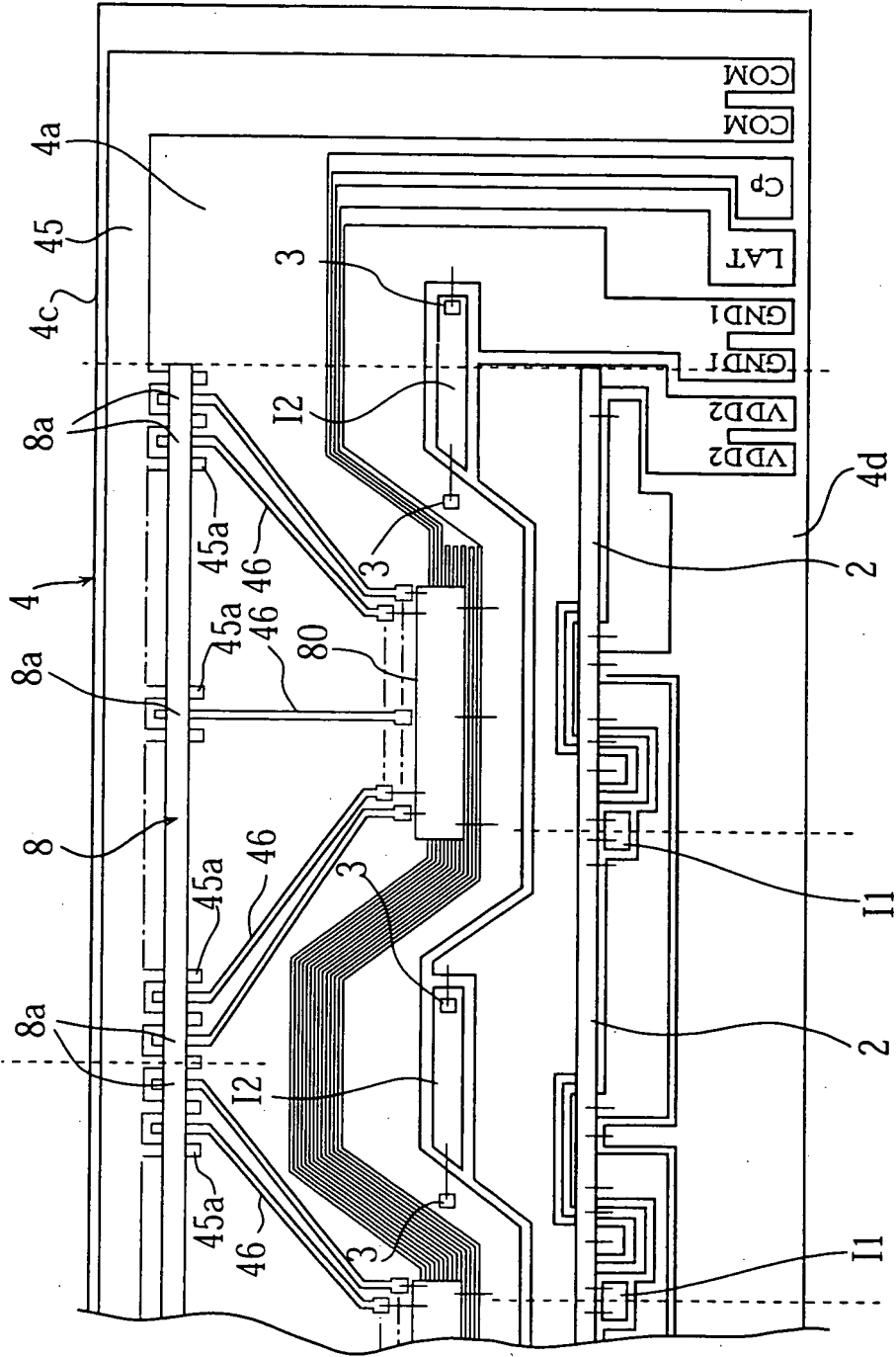


FIG.21

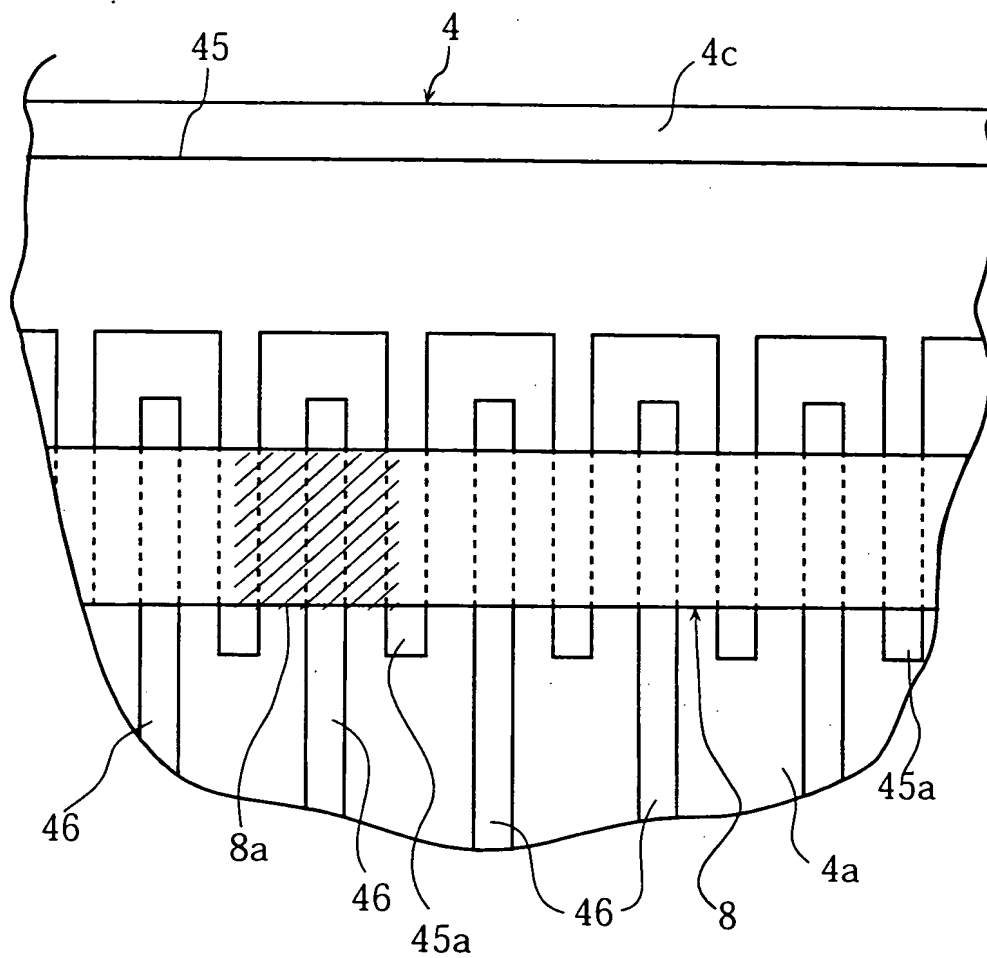
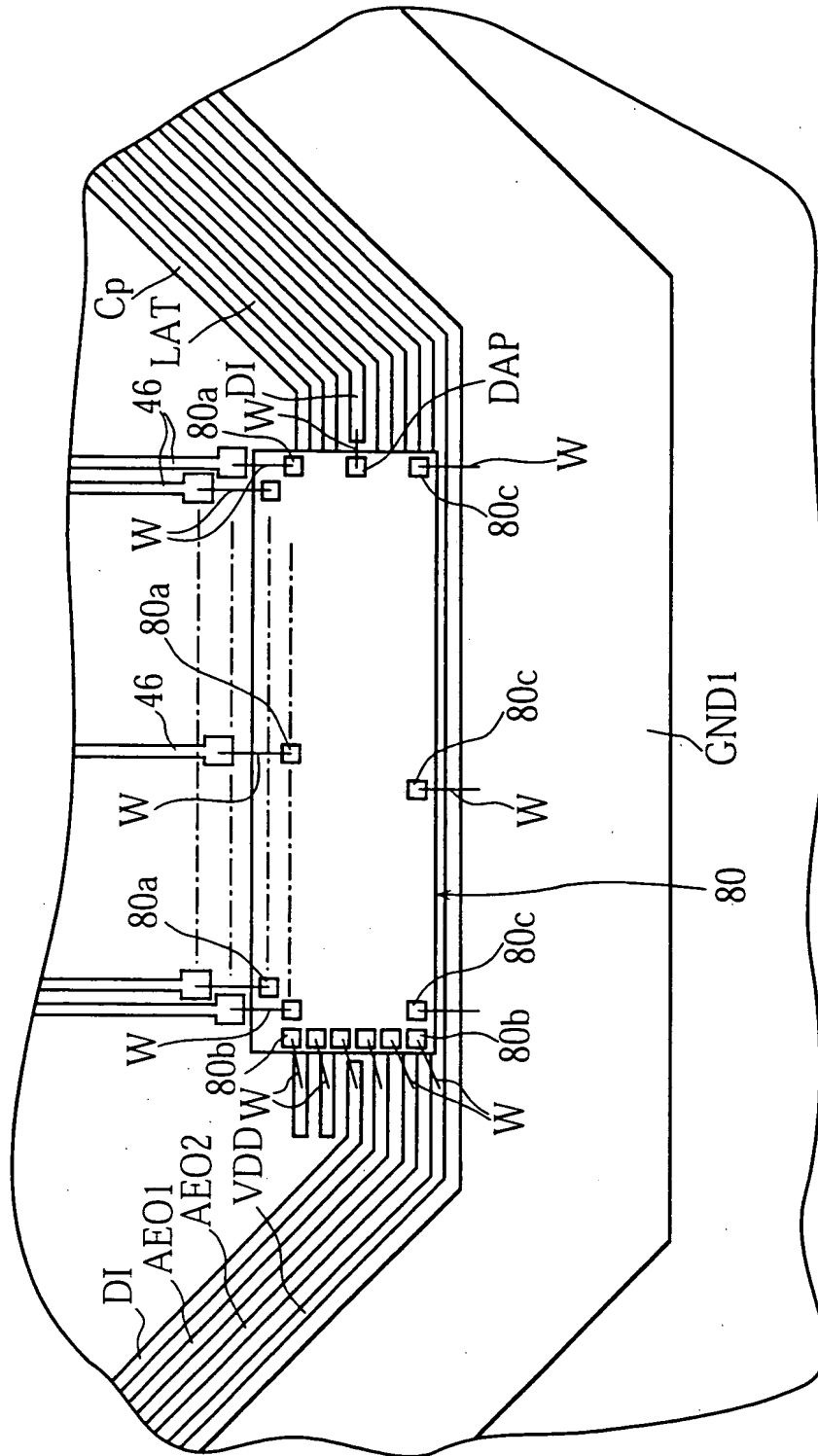


FIG. 22



23/24

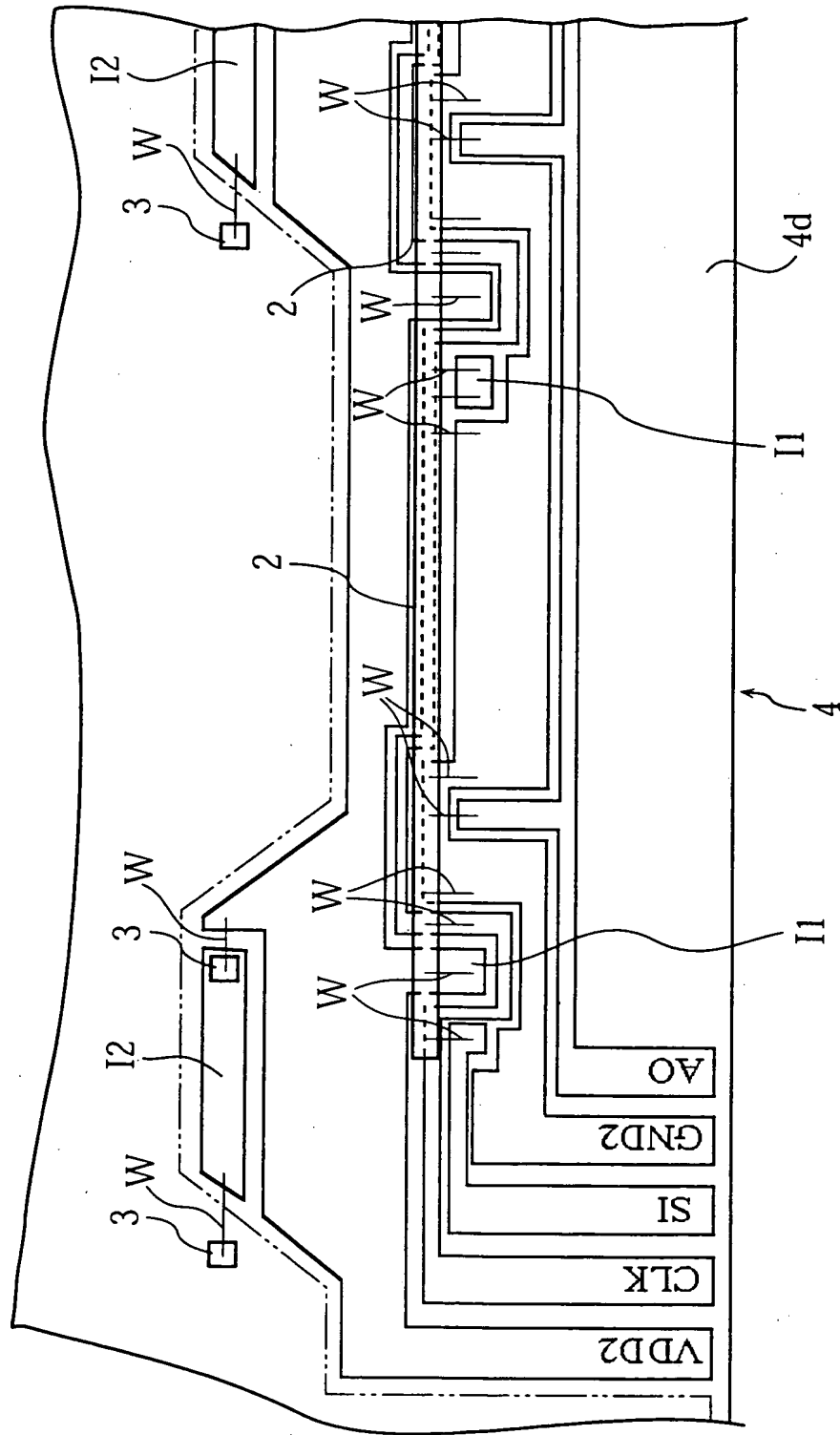


FIG.24

